Amendments to the Specification and Abstract:

Please amend paragraph [0002] beginning on line 13 of page 1 as follows

[0002] In recent years, a width of a gate electrode and a pitch between the gate electrodes has become increasingly ~~narrowed~~ narrow with the achievement of a high degree of integration of a semiconductor device. Specifically, if a process rule is equal to or smaller than 0.18 μm, the minimum space between adjacent gate electrodes is approximately 0.3 μm, which is extremely narrow. As a result, in the case where the above-described narrow space between the adjacent gate electrodes is filled with an interlayer dielectric, there arises a problem of void formation in the interlayer dielectric between the adjacent gate electrodes.

Please amend paragraph [0004] beginning on line 4 of page 2 as follows:

[0004] As a material of the interlayer dielectric for which the above-described heat treatment is performed, it is preferable to use a material which is softened at a low temperature. ~~This is because~~ Because the material softens at a low temperature, transistor characteristics are prevented from being impaired by exposure to an elevated temperature during the heat treatment. For that reason, a boron phosphorous silicate glass (BPSG) film, which reflows at approximately 800 degrees centigrade, is used as the interlayer dielectric. Note that the BPSG film is a dielectric film made out of a silicon oxide film doped with boron (B) and phosphorus (P).

Please amend paragraph [0004] beginning on line 15 of page 2 as follows:

[0005] Hereinafter, referring to the ~~drawing~~ drawings, a conventional method for forming contact holes in a semiconductor device using the above-described BPSG film as an interlayer dielectric is described. FIGS. 5A to 5D are cross section views of a semiconductor device in the process of opening contact holes. Before contact holes are opened through the semiconductor device, transistors are formed on a silicon substrate, and an interlayer dielectric is further formed thereon. Note that a cross section view shown in FIG. 5 illustrates a portion of the semiconductor device which functions as a switching device used in a memory, etc.

Please amend paragraph [0008] beginning on line 17 of page 3 as follows:

[0008] Here, the non-doped oxide film 5 is deposited on the BPSG film 4 for the following reason. The BPSG film 4 is highly hygroscopic. Specifically, when the BPSG film 4 is exposed to the air, boron or phosphorus contained in the BPSG film 4 reacts with water in the air. As a result, compounds of boron, phosphorus, and oxygen, such as BPO_4, B_2O_3, and PO_4, for example, are formed and precipitated on the BPSG film 4. The above-described compounds are foreign substances on the BPSG film 4, and substantially ~~reduces~~ reduce yield in the ~~following~~ subsequent semiconductor device manufacturing process. Thus, the non-doped oxide film 5, which functions as a protective coat, is deposited on the BPSG film 4 so as to prevent the BPSG film 4 from being exposed to the air.

Please amend paragraph [0012] beginning on line 21 of page 4 as follows:

[0012] Note that the gate electrodes 2 of the respective transistors are not formed at regular intervals on the silicon substrate 1. As a result, on the silicon substrate 1, gate electrodes 2 are densely formed in some areas and sparsely formed in other areas. The above-described two types of areas, that is, an area in which the gate electrodes 2 are densely formed and an area in which the gate ~~substrates~~ electrodes 2 are sparsely formed, will ~~arise~~ cause the following problem, which will be described in a concrete manner with reference to the ~~drawing~~ drawings. FIG. 6 is a cross section view of a semiconductor device having an area in which the gate electrodes 2 are densely formed and an area in which the gate ~~substrates~~ electrodes 2 are sparsely formed.

Please amend paragraph [0014] beginning on line 12 of page 5 as follows:

[0014] However, if the gate electrodes 2 are densely formed in some areas and sparsely formed in other areas, the surface of the BPSG film 4 becomes uneven, as shown in FIG. 6, because density of the gate electrodes 2 varies from area to area even after the above-described heat treatment is performed. Specifically, in the area in which the gate electrodes 2 are densely formed, a film thickness De of the BPSG film 4 becomes thick. On the other hand, in the area in which the gate electrodes 2 are sparsely formed, a film thickness Df of the BPSG film 4 becomes

thin. As described above, the heat treatment allows the surface of the BPSG film 4 to be planarized in terms of a local area, such as an area in which the gate electrodes 2 are densely formed or an area in which the gate electrodes 2 are sparsely formed. In terms of the entire area of the semiconductor device, however, the surface of the BPSG film 4 is not planarized. If the non-doped oxide film 5 is deposited on the above-described BPSG film 4 whose surface is not evenly planarized, and the surface of the non-doped oxide film 5 is planarized by means of CMP, a layer composed of the BPSG film 4 and the non-doped oxide film 5 is uniform in thickness, but a thickness ratio of the BPSG film 4 to the non-doped oxide ~~film 4~~ film 5 varies from area to area.

Please amend paragraph [0017] beginning on line 9 of page 7 as follows:

[0017] As shown in FIG. 6, in the area in which the gate electrodes 2 are densely formed, a film ~~thickness~~ of the non-doped oxide film 5 ~~whose~~ (whose etching rate is relatively higher than that of the BPSG ~~film 4~~ film 4) is thicker, and a film ~~thickness~~ of the BPSG film 4 ~~whose~~ (whose etching rate is relatively lower than that of the non-doped oxide ~~film 5~~ film 5) is thinner, compared to the area in which the gate electrodes 2 are sparsely formed. As a result, in the area in which the gate electrodes 2 are densely formed, an etching rate of the interlayer dielectric is higher, compared to the area in which the gate electrodes 2 are sparsely formed. Due to the above-described higher etching rate, the bottom of the contact hole 8e reaches the silicon substrate 1 before the bottom of the contact hole 8f reaches the silicon ~~substrate 1~~ substrate 1, in the case where the contact hole 8e and the contact hole 8f are concurrently ~~opened~~ formed. As a result, the silicon substrate 1 is also etched in the area in which the gate electrodes 2 are densely formed. If the silicon substrate 1 is also etched as described above, a leakage current occurs, which results in a malfunction of the semiconductor device. On the other hand, in the area in which the gate electrodes 2 are sparsely formed, there is a likelihood that the bottom of the contact hole ~~dose~~ will not reach the silicon substrate 1, which results in high incidence of breaks within the semiconductor device.

Please amend paragraph [0024] beginning on line 6 of page 11 as follows:

[0024] After planarization of the first dielectric film, the second dielectric film is preferably

deposited thereon before formation of a precipitate on the surface of the first dielectric film ~~for the reason that~~ because the above-described precipitate ~~interferes~~ will interfere with the uniform deposition of the second dielectric film. Specifically, the second dielectric film is preferably deposited within 24 hours after planarization of the first dielectric film.

Please amend paragraph [0027] beginning on line 21 of page 11 as follows:

[0027] Furthermore, it is possible to apply the present aspect to a case ~~of where~~ in which the contact holes are formed in a semiconductor device having an area in which interconnections are densely formed and an area in which interconnections are sparsely formed, or a case ~~where in~~ which the contact holes are formed in a semiconductor device on which a plurality of interconnections of different widths are formed.

Please amend paragraph [0031] beginning on line 10 of page 13 as follows:

[0031] Hereinafter, referring to the drawings, a contact hole formation method according to a first embodiment of the present invention will be described. According to the contact hole formation method of the present embodiment, contact holes are opened in a semiconductor device having a silicon substrate on which an interlayer dielectric film composed of a BPSG film layer and a non-doped oxide film layer is deposited. A main feature of the contact hole formation method of the present embodiment is that the BPSG film and the non-doped oxide film, which are deposited on the silicon substrate, are planarized, whereby contact holes of uniform depth can be opened even if the semiconductor device has an area in which gate electrodes of a transistor are densely formed and an area in which gate electrodes are sparsely formed. Here, FIGS. 1A to 1E are cross section views of a semiconductor device in the process of having contact holes opened therein. The semiconductor device shown in FIG. 1 includes the silicon substrate, and transistors formed thereon, and an interlayer dielectric further formed thereon. Note that a cross section views shown in FIG. 1 illustrates a portion of the semiconductor device which functions as a switching device used for a memory, etc.

Please amend paragraph [0035] beginning on line 2 of page 15 as follows:

[0035] Next, as shown in FIG. 1B, the surface of the BPSG film 4 is planarized by means of

CMP. For performing the above-described CMP, various conditions such as processing time, etc., are adjusted so that a film thickness of the planarized BPSG film 4 becomes approximately 600 nm. The CMP allows the BPSG film 4 to have a uniform thickness, irrespective of whether or not there is ~~the~~ a gate electrode 2 on the silicon substrate 1, by global planarization of the surface of the BPSG film 4. Note that the above-described process is a main feature of the present invention.

Please amend paragraph [0036] beginning on line 11 of page 15 as follows:

[0036] Next, as shown in FIG. 1C, the non-doped oxide film 5 is deposited on the surface of the BPSG film 4, which ~~is~~ has been planarized by means of CMP. Specifically, the TEOS film, whose film thickness is approximately 50nm, is deposited by means of CVD. Here, when the surface of the BPSG film 4 is exposed to the air, boron or phosphorus contained in the BPSG film 4 reacts with water in the air. As a result, compounds such as BPO_4, B_2O_3, and PO_4, for example, are formed and precipitated on the surface of the BPSG film 4. The above-described compounds are foreign substances on the surface of the BPSG film 4, and substantially reduce yield in the ~~following~~ subsequent semiconductor device manufacturing process. Thus, the non-doped oxide film 5, which functions as a protective coat, is deposited on the BPSG film 4.

Please amend paragraph [0038] beginning on line 15 of page 16 as follows:

[0038] As shown in FIG. 2, the number of foreign substances is sharply increased after a lapse of 48 hours after planarization of the BPSG film 4. Thus, in this embodiment, allowing for a margin of a certain amount of time, the non-doped oxide film 5 (for example, a TEOS film) is deposited within about 24 hours after planarization of the BPSG film 4 by means of CMP. As a result, it is possible to prevent the formation of foreign substances on the planarized BPSG film 4, and to deposit the non-doped oxide film 5 so as to be more uniform than before.

Please amend paragraph [0043] beginning on line 24 of page 17 as follows:

[0043] As aforementioned, in the present embodiment, the non-doped oxide film 5 is deposited on the planarized BPSG film 4, and the non-doped oxide film 5 is also planarized. Thus, it is possible to form the BPSG film 4 and the non-doped oxide film 5 each having a uniform

thickness over the entire area of the semiconductor device as shown in FIG. 3, irrespective of whether the gate electrodes 2 formed on the silicon substrate 1 are densely or sparsely distributed. Specifically, a film thickness Da of the BPSG film 4 in an area in which the gate electrodes 2 are densely formed is equal to a film thickness Db of the BPSG film 4 in an area in which the gate electrodes 2 are sparsely formed, and a film thickness da of the non-doped oxide film 5 in the area in which the gate electrodes 2 are densely formed is equal to a film thickness db of the non-doped oxide film 5 in the area in which the gate electrodes 2 are sparsely formed. Thus, it is possible to equalize an etching rate of the interlayer dielectric (in this embodiment, a dielectric layer composed of the BPSG film 4 and the non-doped oxide film 5) over the entire area of the semiconductor device. As a result, it is possible to open a plurality of contact holes of uniform depth in the entire area of a dielectric film by means of dry etching. The above-described dielectric film is composed of more than 1 type of dielectric film each having different etching rates, and deposited on the silicon substrate 1 having an area in which the gate electrodes 2 are densely formed and an area in which the gate electrodes 2 are sparsely formed. Thus, the contact hole formation method according to the present embodiment can prevent the following adverse phenomenon, for example, a phenomenon in which leakage of current occurs because the substrate is also etched due to an increased etching rate in an area in which the gate electrodes 2 are densely formed, or a phenomenon in which an interconnection between the semiconductor device and its lower layer tends to be broken because the bottom of the contact hole does not reach the substrate due to a reduced etching rate in an area in which the gate electrodes 2 are sparsely formed.

Please amend paragraph [0053] beginning on line 23 of page 22 as follows:

[0053] After completion of cleaning of the surface of the BPSG film 4, the non-doped oxide film 5 is deposited on the surface of the BPSG film 4 as shown in FIG. 1C. Specifically, the TEOS film, whose film thickness is approximately 50nm, is deposited by means of CVD. Here, when the surface of the BPSG film 4 is exposed to the air, boron or phosphorus contained in the BPSG film 4 reacts with water in the air. As a result, the compounds such as BPO_4, B_2O_3, and PO_4, for example, are formed and precipitated on the surface of the BPSG film 4. The above-described compounds are foreign substances on the surface of the BPSG film 4, and substantially

reduce yield in the ~~following~~ subsequent semiconductor device manufacturing process. Thus, the non-doped oxide film 5, which functions as a protective coat, is deposited on the BPSG film 4. Note that the above-described process is also identical to that of the first embodiment.

Please amend paragraph [0057] beginning on line 8 of page 24 as follows:

[0057] As described above, according to the contact hole formation method of the present embodiment, even if compounds are precipitated on the surface of the BPSG film 4 after a predetermined time period (for example, 24 hours or more) has elapsed after planarization of the BPSG film 4, it is possible to eliminate the compounds precipitated on the surface of the BPSG film 4. As a result, the non-doped oxide film 5 can be uniformly deposited. That is, it is not necessary to control the time elapsed after planarization of the BPSG film 4 because foreign substances on the surface of the BPSG film 4 are reliably eliminated. Thus, even if the wafer is left untouched after deposition of the BPSG film 4 for a predetermined time period, and compounds are precipitated on the surface of the BPSG film 4 during the predetermined time period before deposition of the non-doped oxide film 5, it is possible to form contact holes of uniform depth, thereby preventing yield from being reduced in the ~~following~~ subsequent semiconductor device manufacturing process.

Please amend paragraph [0057] beginning on line 8 of page 24 as follows:

[0061] Note that, in the first and second embodiments, the contact holes are opened between the gate electrodes of the ~~transistor, but~~ transistor. However, the contact holes may be opened in other places. For example, the contact holes may be opened on the respective gate electrodes, or may be opened on respective gate electrode interconnections 12 as shown in FIG. 4. Here, the gate electrode interconnection 12 is an interconnection formed on an STI (Shallow Trench Isolation) dielectric film 11 on the silicon substrate 1, and the gate electrode interconnection 12 is connected to a gate electrode of the transistor. Also in this case, the gate electrode interconnections 12 are densely formed in some areas and sparsely formed in other areas, whereby there arises the same problem as the one which arises in the case of the gate electrode 2. However, the contact hole formation method according to the present invention allows the contact holes of uniform depth to be opened on the respective gate electrode interconnections 12,

as is the case with the gate electrode 2.